during [a] each of said LOAD [period] periods and when a select line signal on the select line activates the control circuit, said data line supplies a data signal to the control circuit where said data signal is stored; and

during [an] each of said ILLUMINATE [period] periods, in response to a state of said stored data signal, said control circuit applies pulsed energy from a power supply means to a second electrode of said electroluminescent cell for a particular period of time.

In claim 27, line 1 Change "26" to --20--.

30. (amended) An electroluminescent display comprising an array of pixels, each pixel comprising:

a first transistor, a second transistor and an electroluminescent cell;

said first transistor having a first transistor gate connected to a select line, a first transistor source connected to a data line, and a first transistor drain connected to connected to a second transistor gate of said second transistor;

said second transistor having a second transistor source connected to said [data] select line and a second transistor drain coupled to a first electrode of said electroluminescent cell; and

said electroluminescent cell having a second electrode coupled to means for providing an alternating current to the electroluminescent cell.

REMARKS

In view of both the amendments presented above and the following discussion, the applicant submits that none of the claims now pending in the application is obvious under the provisions of 35 U.S.C. § 103. Thus, the applicant believes that all of these claims are now in allowable form.

Recapture of Canceled Subject Matter

The Examiner contends that the new claims (claims 8-32) of this application "recapture" the invention recited in claims 8-13 of the application that resulted in the issued patent (U.S. application number 07/892,464). The applicant respectfully disagrees.

Specifically, original claims 8-13 (the '464 claims) recited a particular pixel circuit structure that accomplished the method of the invention. In contrast, the reissue claims 8-13 do not recite a specific circuit structure of the pixel. Since reissue claims 8-13 do not recite the same subject matter as the claims 8-13 of the '464 application, the reissue claims do not recapture the subject matter of the deliberately canceled claims of the '464 application.

Furthermore, claims 8-29, as amended, contain the limitation of using a frame period that is divided into a plurality of successive LOAD and ILLUMINATE periods. As such, the present invention, as recited in claims 8-29, repetitively applies energy to the EL cell to achieve illumination that depicts a frame of image data. This limitation was not recited in the '464 claims.

As for claims 30-32, these claims recite an embodiment of the invention having the first transistor gate and the second transistor source connected to the select line. In contrast, the '464 claims did not recite this specific embodiment of the invention.

Therefore, the claims of the Reissue application do not recapture recitations made in the '464 claims and, as such, the applicant submits that the reissue should be granted for this patent.

Rejections

A. Defective Reissue Declaration

The Examiner has rejected claims 1-32 because the claims were based upon a defective reissue declaration under 35 U.S.C. § 251.

In response, the applicant has attached hereto a supplemental declaration that corrects the deficiencies of the original declaration delineated by the Examiner. Additionally and in support of the applicant's statements in the supplemental declaration, the applicant includes an affidavit from the undersigned attorney, Mr. Raymond R. Moser Jr., Esq., that reviewed the original patent and initiated the reissue application.

B. 35 U.S.C. § 103

The Examiner has rejected claims 8-32 as being unpatentable over the Asars patent (United States patent 4,087,792 issued May 2, 1978). The rejection is respectfully traversed.

The Examiner contends that Asars discloses a method of operating an electroluminescent (EL) display by applying voltages to select and data lines to select a particular pixel for illumination, forming a signal representative of gray scale information, and applying the signal to the means for controlling, e.g. a transistor. The Examiner also contends that Asars discloses "circuitry that employs analog signals and disables the means during a first part and second part of a period of time". However, the Examiner concedes that Asars does not disclose "digital signals involving bits", but the Examiner contends that the use of digital signals is well-known. Consequently, the Examiner concludes that the teachings of Asars combined with the skill in the art teaches the applicant's invention. The applicant respectfully disagrees.

Asars teaches, as depicted in FIG. 1 thereof, an EL display having a plurality of pixels, where each pixel is controlled by a transistorized control circuit. The control circuit comprises two transistors. The first transistor has a gate terminal connected to a first bus line (select line), a source terminal connected to a second bus line (data line), and a drain terminal connected to a gate terminal of a second transistor. The second transistor has a drain terminal connected to an EL cell and a source terminal to a

SOURCE signal input. The first and second bus lines are used to select a particular pixel for illumination and to apply a certain voltage to a capacitor connected to the gate terminal of the second transistor. To illuminate a particular EL cell, a ramp voltage is applied to the SOURCE signal input. A ramp voltage is shown in FIGS 2A, 2B, 3A and 3B. The amount of EL cell illumination is determined by the relative values of the ramp voltage and the voltage at the gate of the second transistor. For a particular voltage at the gate of the second transistor (e.g., the voltage to which the gate capacitor is charged), the EL cell illuminates for a particular period of time during the ramp voltage, e.g., illumination occurs while the ramp voltage is greater than the gate voltage or vice versa. Thus, gray scale illumination control is achieved by applying various voltage levels to the gate capacitor from the second bus (data line). To produce a gray scale image, one cycle of ramp voltage is applied to the control circuitry for each frame of image information.

The applicant's invention operates in a substantially different manner than that taught by Asars. For example, claim 8 recites:

> "In an electroluminescent display comprising an array of pixels, where each pixel contains a circuit for controlling application of energy to an electroluminescent cell associated with each pixel in said array of pixels, a method of providing gray scale illumination during a frame period comprising the steps of:
>
> dividing said frame period into a plurality of LOAD periods and a plurality of ILLUMINATE periods, where each LOAD period is followed by an ILLUMINATE period;
>
> applying, during each of said LOAD periods, a data signal to said circuit along a data line and applying a select signal to said circuit along a select line;
>
> storing, during each of said LOAD periods, said data line signal within said circuit; and

> applying, during each of said ILLUMINATE periods, a current to said electroluminescent cell and said circuit, where said electroluminescent cell is selectively illuminated in response to said current and said stored data line signal." (emphasis added).

The emphasized portion of claim 8 highlights a step in the applicant's method that is not taught by Asars. Specifically, this step involves dividing a frame period into a plurality of successive LOAD and ILLUMINATE periods. As such, to achieve gray scale illumination during a frame period, the plurality of LOAD and ILLUMINATE periods must be accomplished. The need for successive LOAD and ILLUMINATE periods during one frame arises because the applicant's invention does not use a SOURCE signal as required by Asars. Specifically, Asars teaches using a constant gate capacitor voltage and a varying SOURCE signal to achieve gray scale illumination during a frame period, while the present invention uses a variable gate capacitor voltage that can change during each LOAD period of a given frame period and a fixed source terminal signal (i.e., there is no SOURCE signal per se). Since there is no teaching in Asars that suggests that the SOURCE signal is optional, there is no reason for a person skilled in the art to modify the Asars invention to attain the applicant's invention. As such, the teachings of Asars in view of the skill in the art would not result in the applicant's invention as recited in claim 8.

The applicant's other independent method claims (claims 14 and 20) include a similar recitation to that in claim 8 above. That is, each independent claim recites dividing a frame period into a plurality of successive LOAD and ILLUMINATE periods.

Therefore, the applicant submits that claims 8, 14, and 20, as they now stand, fully satisfy the requirements of 35 U.S.C. § 103 and are patentable thereunder.

Furthermore, dependent claims 9-13, 18-19, and 22-25 depend, either directly or indirectly, from claims 8, 14, and 20 and recite additional features therefor. As such and for the exact

same reasons set forth above, the applicants submit that none of these claims is obvious with respect to the teachings of Asars in view of the skill in the art. Therefore, the applicants submit that all these dependent claims also fully satisfy the requirements of 35 U.S.C. § 103 and are patentable thereunder.

As for claims 30-32, these claims recite, in part:

"a first transistor, a second transistor and an electroluminescent cell;

said first transistor having a first transistor gate connected to a select line, a first transistor source connected to a data line, and a first transistor drain connected to connected to a second transistor gate of said second transistor;

said second transistor having a second transistor source connected to said select line and a second transistor drain coupled to a first electrode of said electroluminescent cell; and

said electroluminescent cell having a second electrode coupled to means for providing an alternating current to the electroluminescent cell." (emphasis added).

This circuit structure for a pixel (e.g., having a second transistor source connected to the select line as emphasized above) is neither taught nor suggested by the cited prior art. Therefore, the applicants submit that claims 30-32 fully satisfy the requirements of 35 U.S.C. § 103 and are patentable thereunder.

Conclusion

Thus, the applicant submits that none of the claims, presently in the application, is obvious under the provisions of 35 U.S.C. § 103. Consequently, the applicants believe that all these claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If, however, the Examiner believes that there are any unresolved issues requiring adverse final action in any of the

claims now pending in the application, it is requested that the Examiner telephone Mr. Raymond R. Moser Jr., Esq. at (908) 530-9404 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

Respectfully submitted,

8-16-96

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CERTIFICATE OF MAILING under 37 C.F.R. § 1.8(a)

I hereby certify that this correspondence is being deposited on 8-16-96 with the United States Postal Service as first class mail, with sufficient postage, in an envelope addressed to the Commissioner of Patents and Trademarks, Washington, D.C. 20231.

Allyson M. DeVesty
Signature

Allyson M. DeVesty
Name